Chips with everything

"Chips glorious chips"

26 July 2011

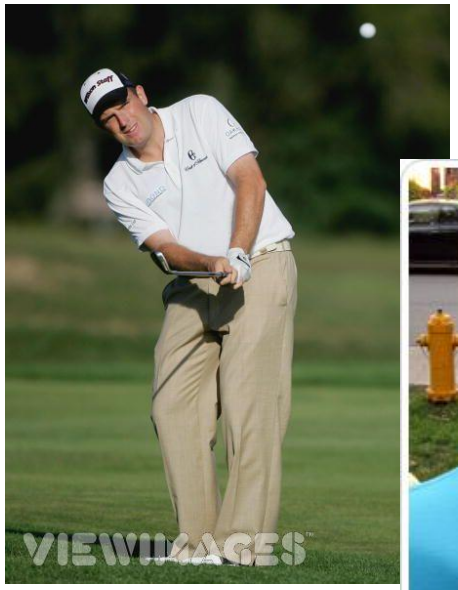
Farah Khalid
Microelectronics

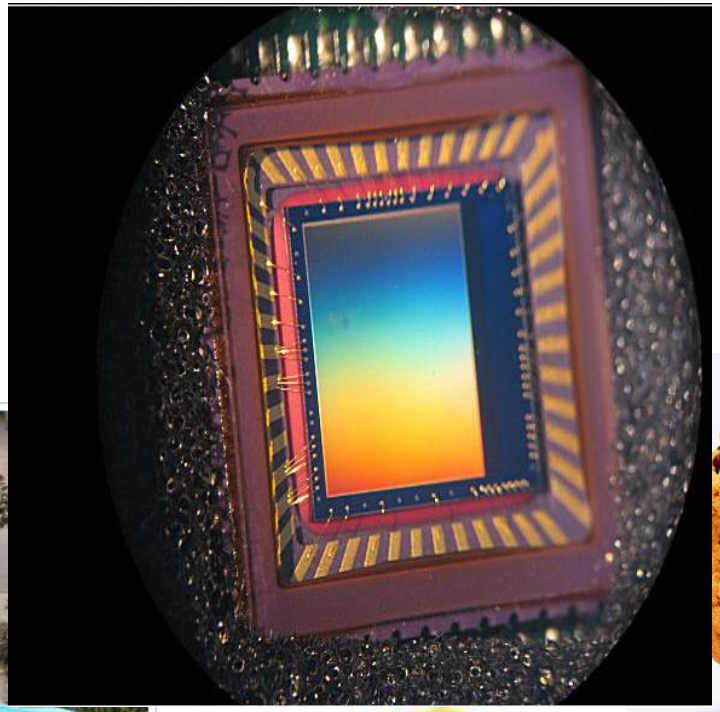
Scope of Presentation

1. What is a chip?
2. History
3. Where do we use chips?
4. Making Chips – System Design
5. Making Chips – Physical Design
6. Industry Trends
7. 3D Chips

WHAT IS A CHIP?

What is a chip??



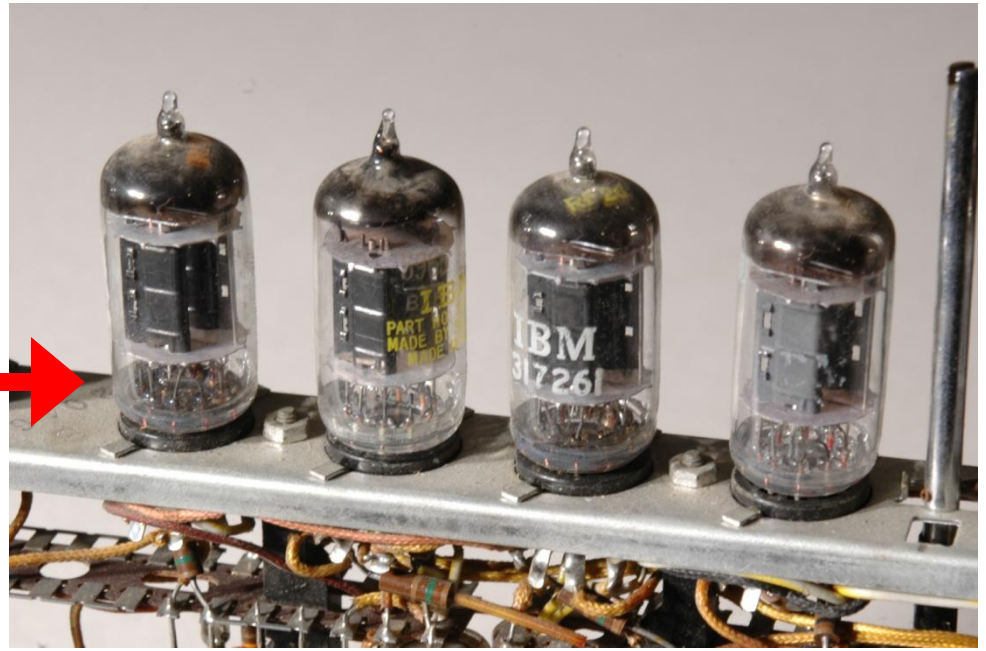


"Chip"
APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC)

Integrated circuit is a miniaturized electronic circuit consisting of transistors, resistors and capacitors.

HISTORY: How did we get here??

HISTORY

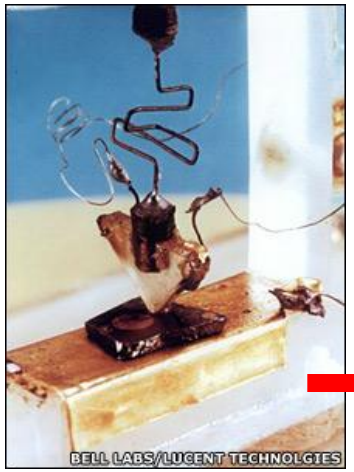


First electronic components allowing performing nonlinear funnctions were vacuum tubes

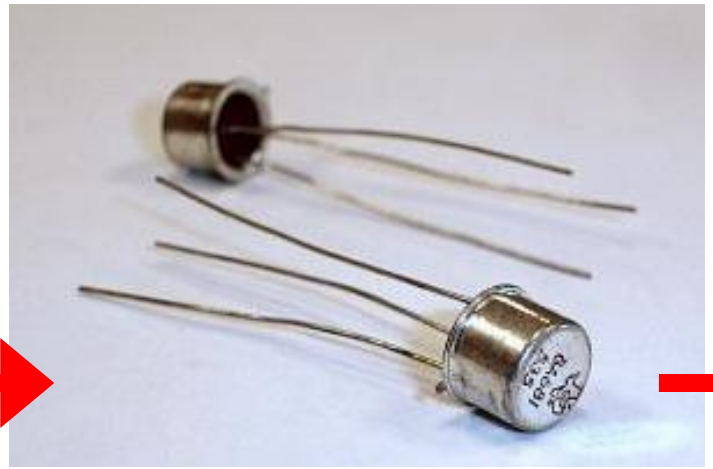
Construction of vacuum tubes was complex, their cost was high, but above all they were bulky (not good candidates for miniaturization)

They are still loved by audiphiles for highest fidelity in sound

HISTORY

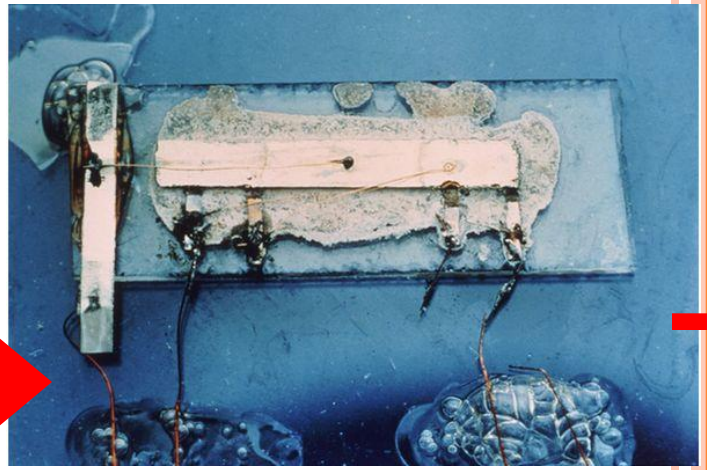


First transistor
(Bell Labs 1947)

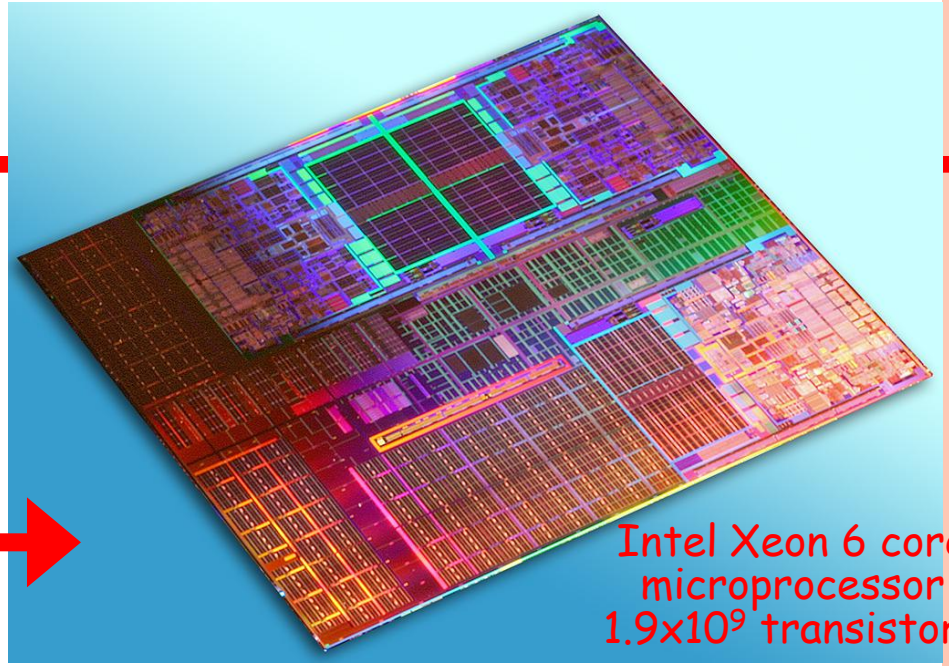


Very soon we have two
and more transistors

First integrated circuit
(Texas Instruments 1958)



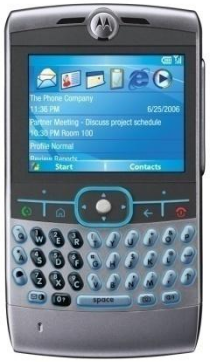
More and more components, more and
more functions, growing complexity



Intel Xeon 6 core
microprocessor
1.9×10^9 transistors

Where are chips used?

Where are chips??



What else can we do with chips??

Medical Applications:

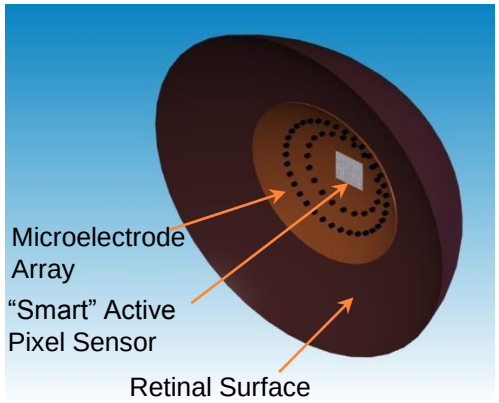
Medical Imaging

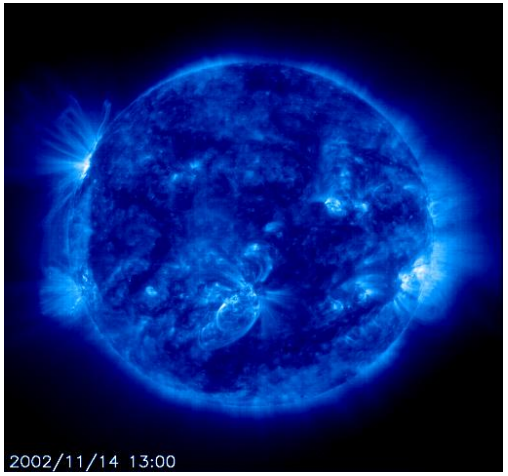
Retinal Implant

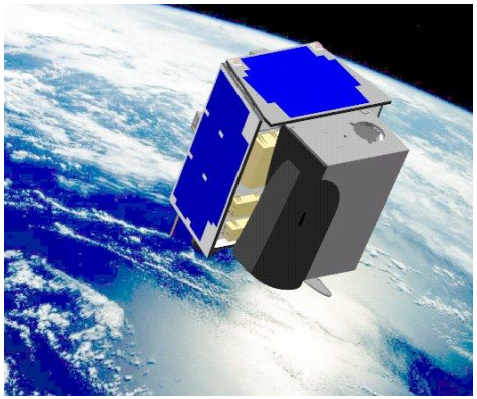
Astrophysics:

Earth Observation

Solar Orbiter



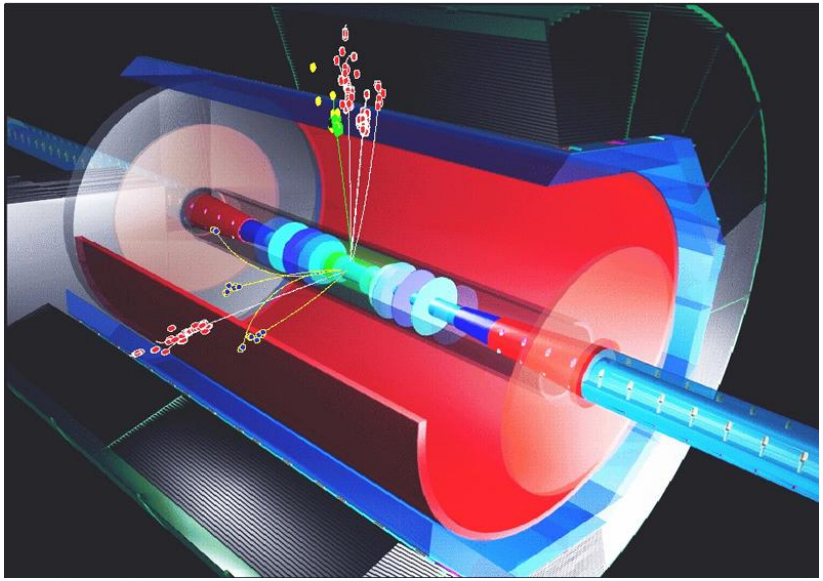


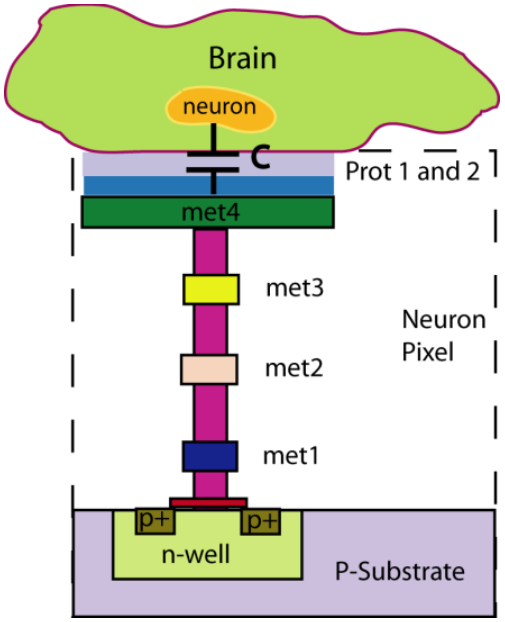


What do we do with chips??

Neuron Imaging

High Energy Physics





SYSTEM DESIGN

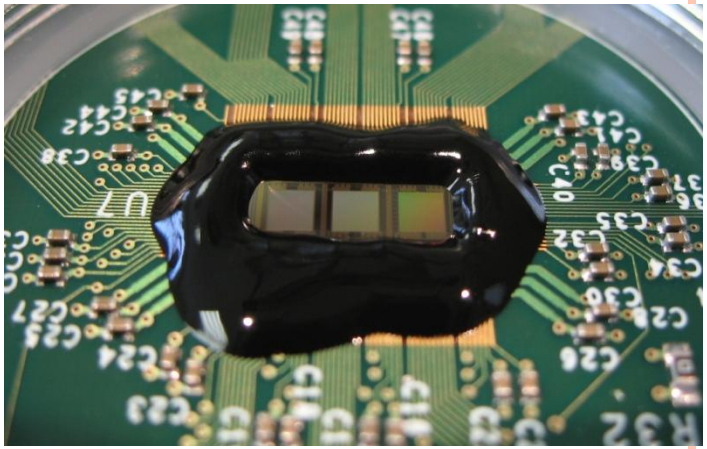
System Design

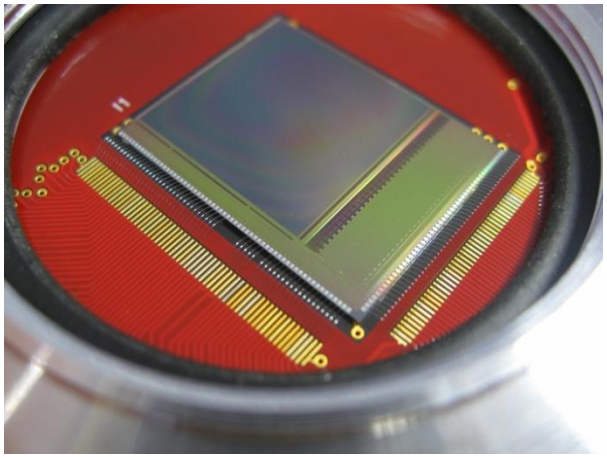
- Requirements Analysis
- Existing system performance & physical constraints
- System architecture
- Design specification
- Design & Manufacture
- Test
- System Test

System Design

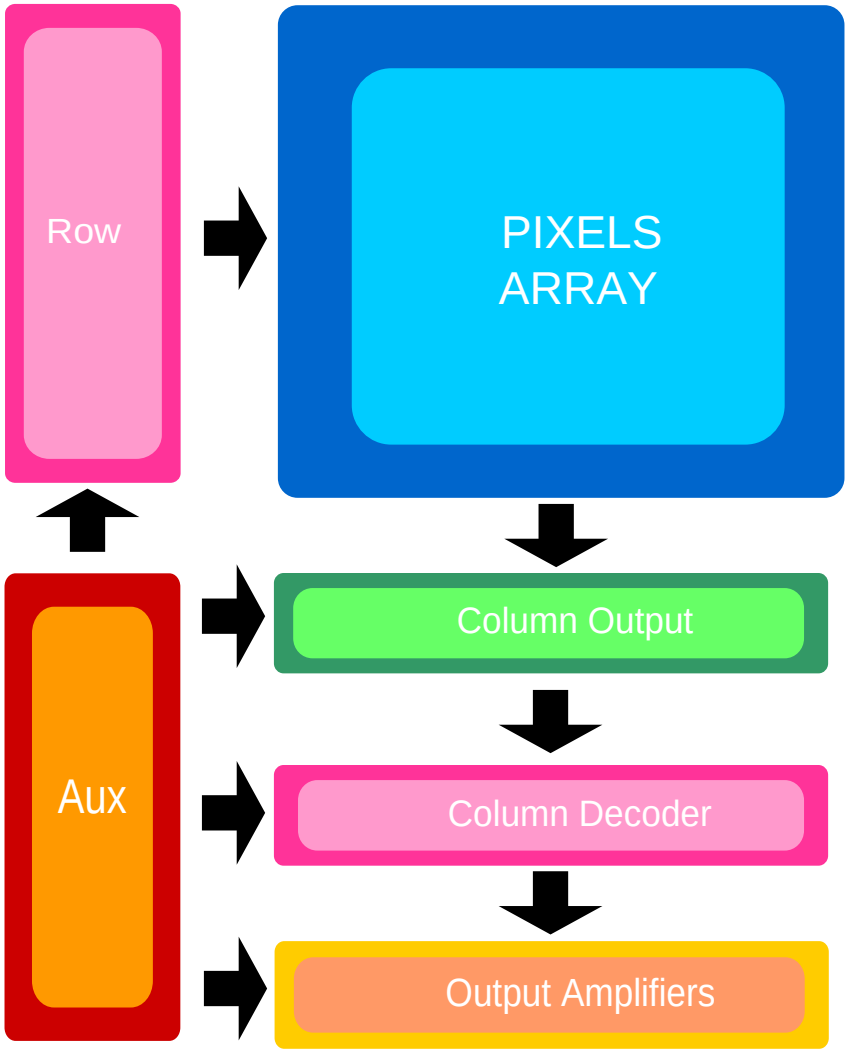
Once the needs for the chosen application have been identified it is possible to design a system around the chip.

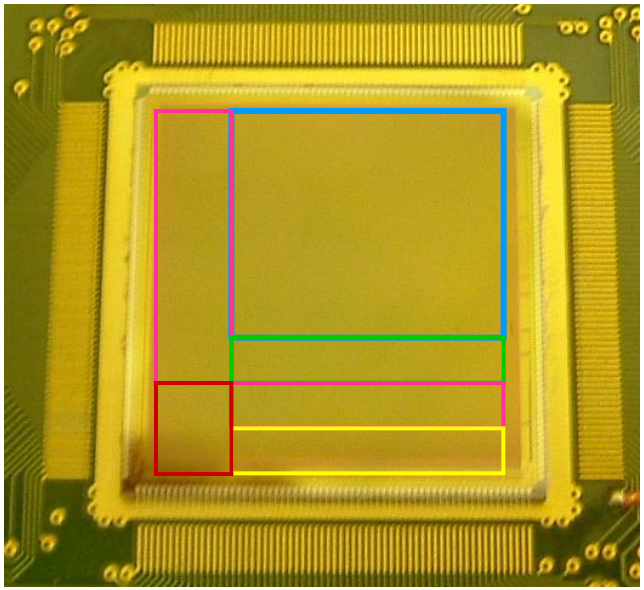
The system will include all the components required to form a working prototype.





Chip Design

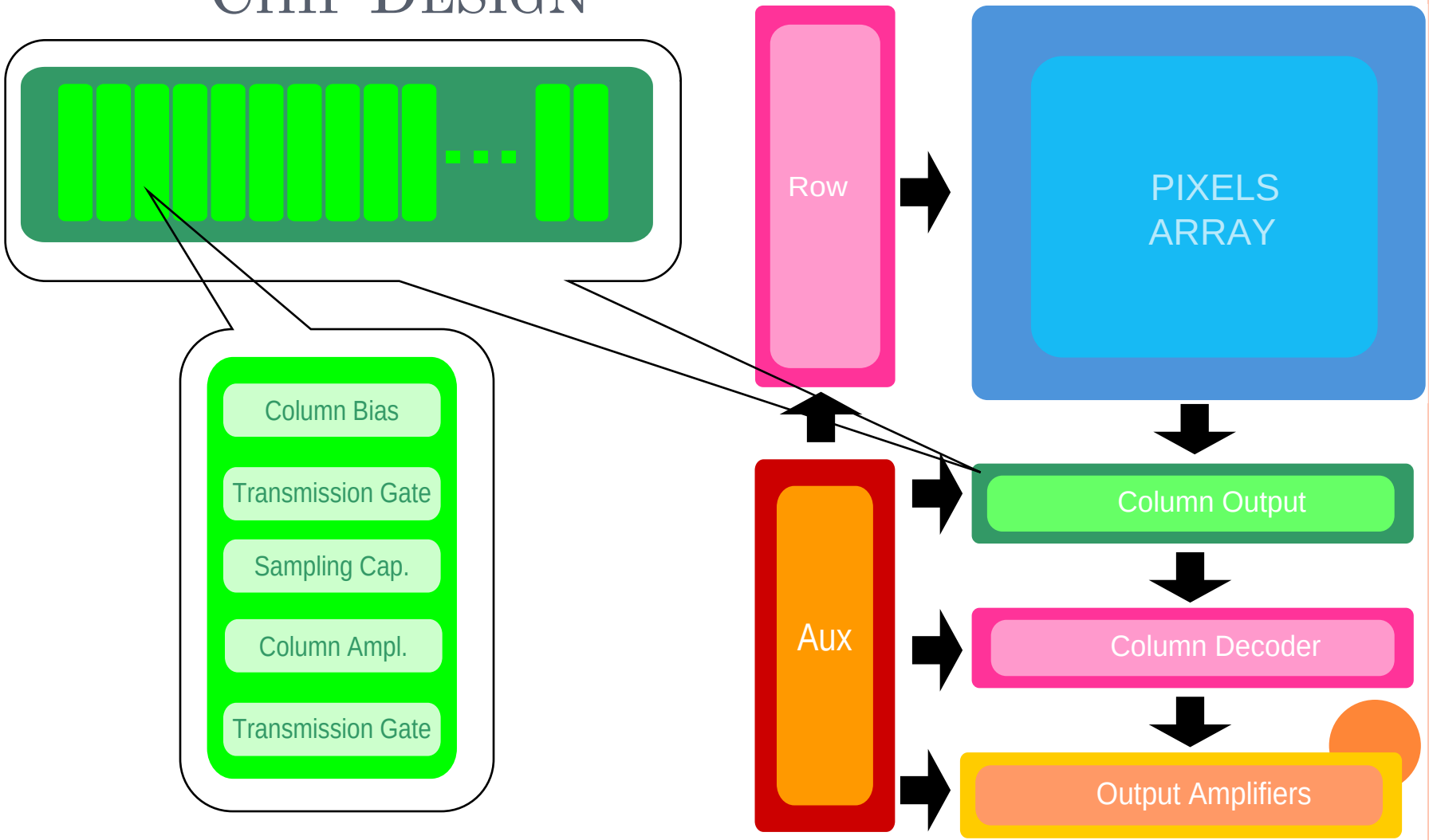




Normally the “chip” is divided into several different sub-blocks.

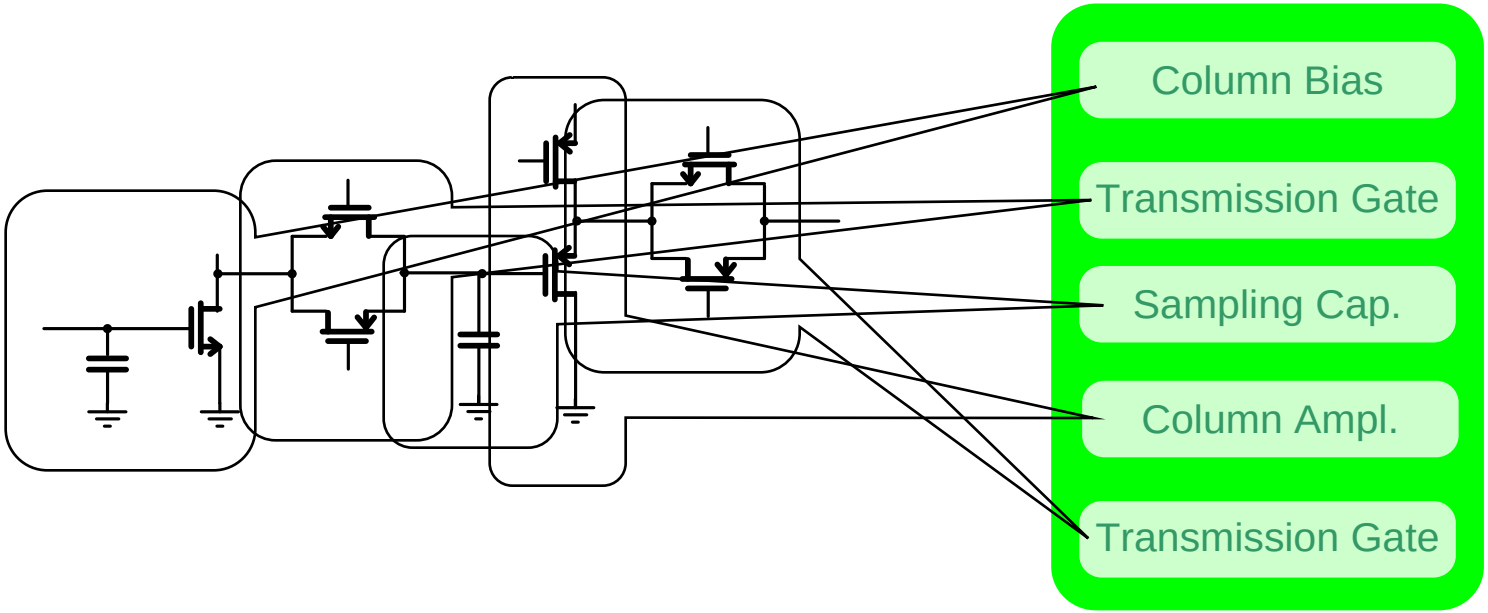
TOP-DOWN

Chip Design


Row
PIXELS ARRAY
Column Bias
Transmission Gate
Sampling Cap.
Column Ampl.
Transmission Gate
Aux
Column Output
Column Decoder
Output Amplifiers

Chip Design

The “basic building blocks” are transistors, capacitors, resistors and diodes.

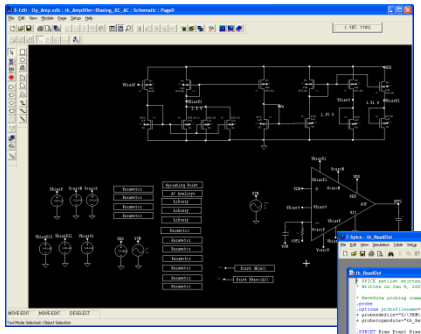


Such blocks are modelled with a mathematical equivalent of each component to enable the evaluation of the behaviour of a circuit using a PC/workstation.

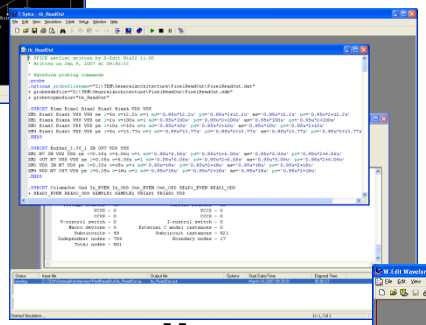
Design Flow

Chip design flow can be divided in 5 steps.

BOTTOM-UP

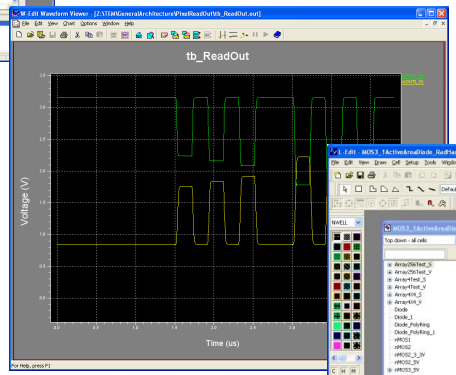


Schematic

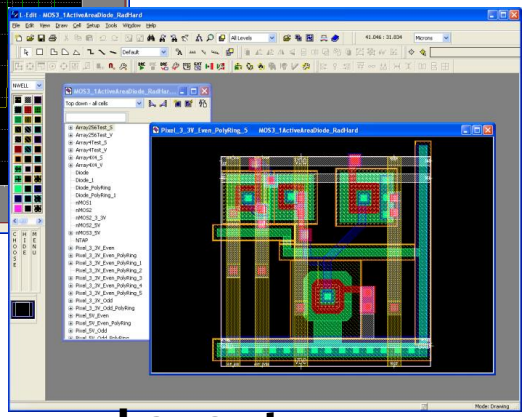


Netlist

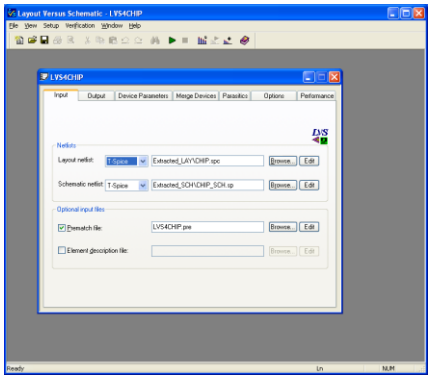
Backannotation



Simulation

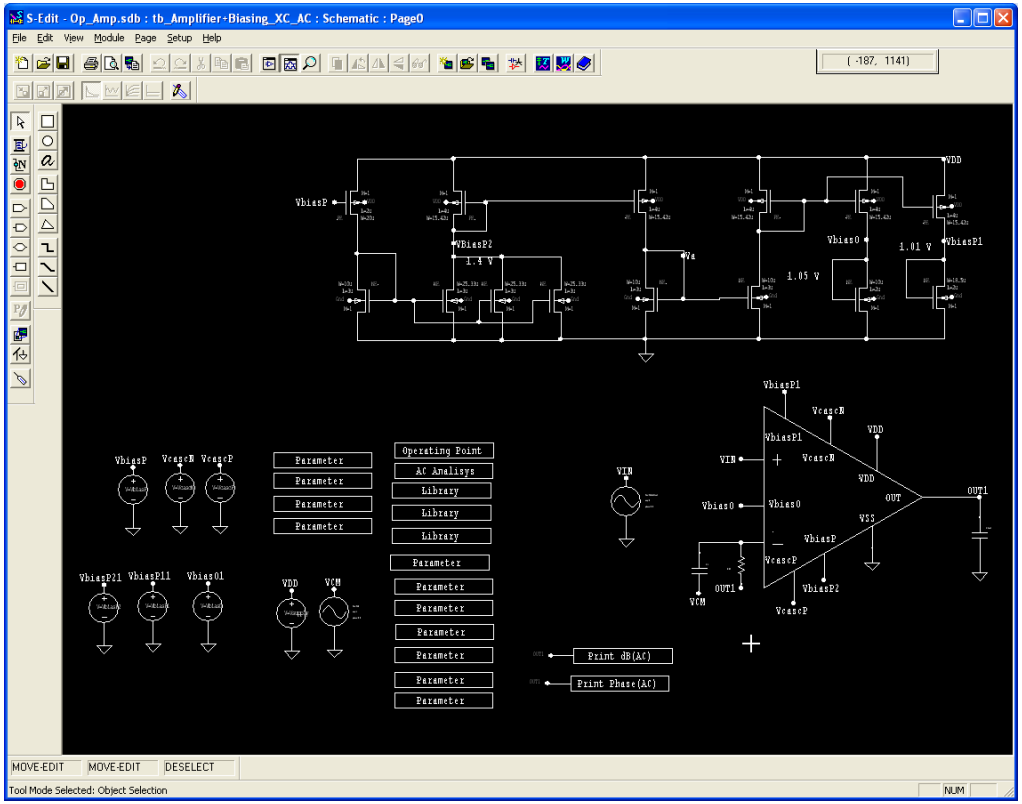


Layout



LVS

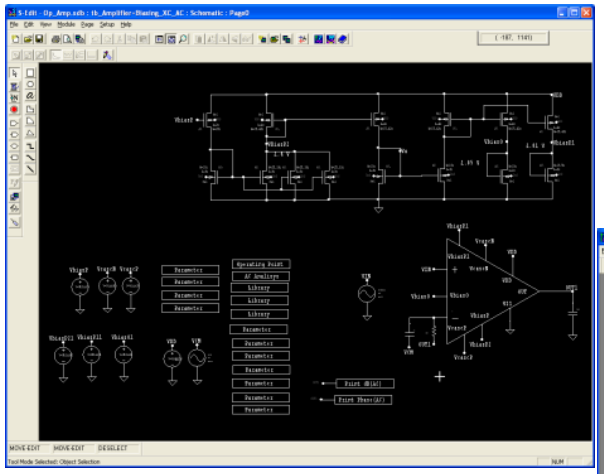
Schematic



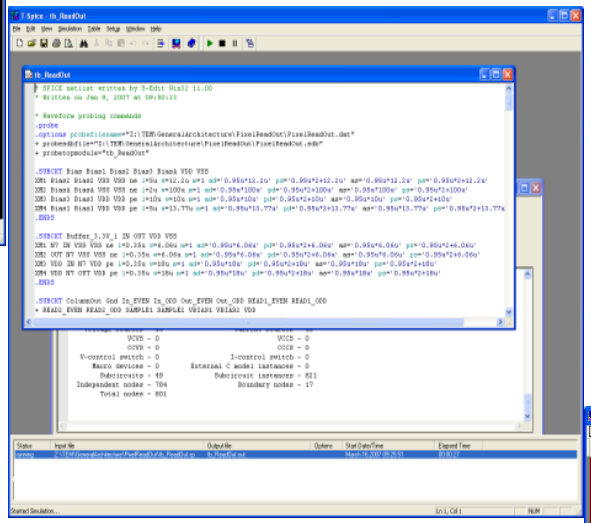
The different circuit components and their connectivity have to be entered in the schematic in order to be evaluated (simulated).

It is possible to define hierarchical blocks to save time and obtain compact designs.

Design Flow

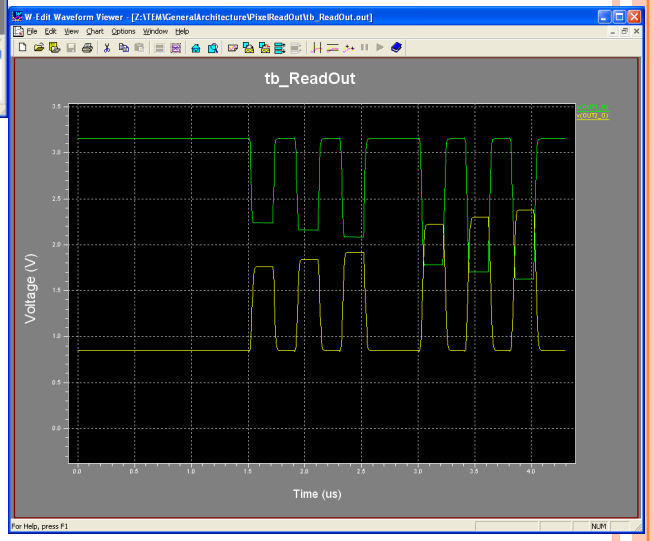


Schematic



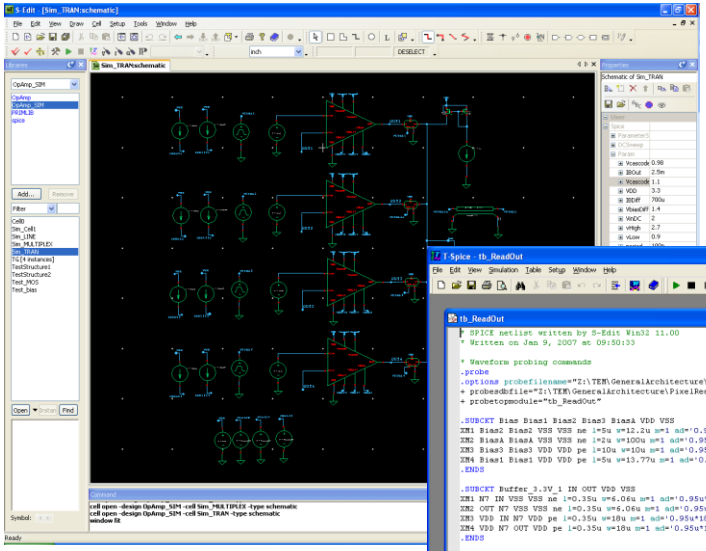
Netlist

Simulation

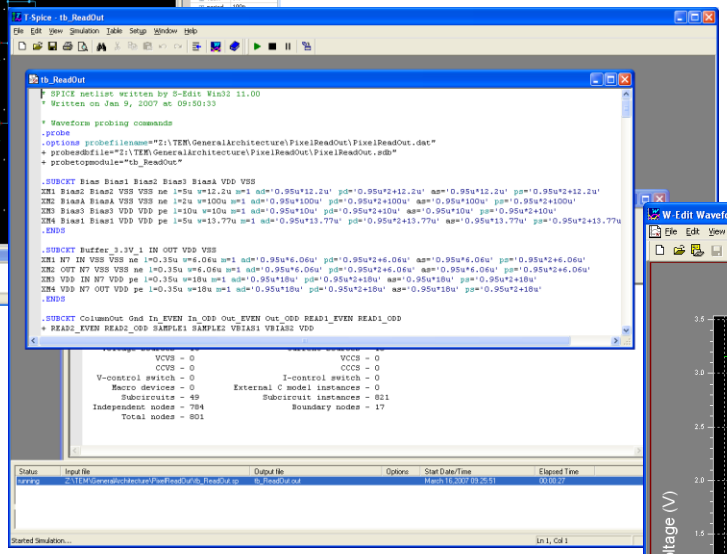


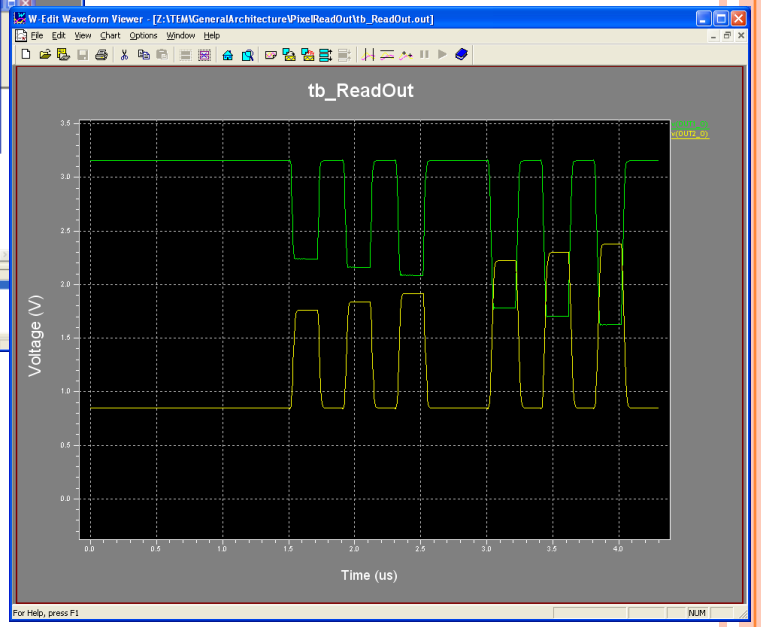
Simulation

It is possible to evaluate the response of the circuit by adding some instructions to the schematic



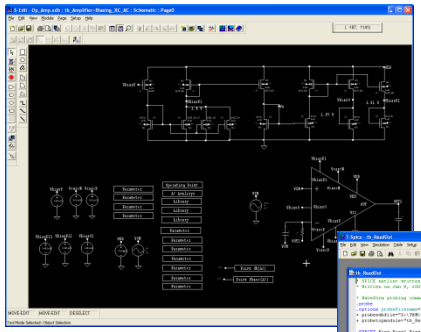
- Large signal Analysis: Transient (time response)
- Small signal Analysis: AC (frequency response)
- Noise Analysis



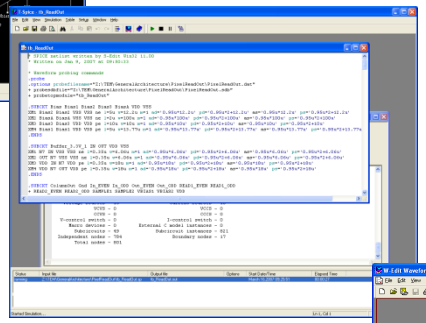


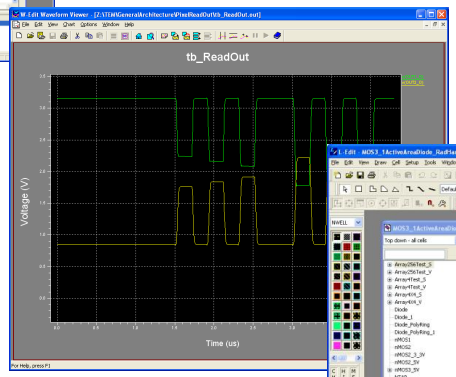
Process, temperature, mismatched components are all taken into consideration.

Design Flow



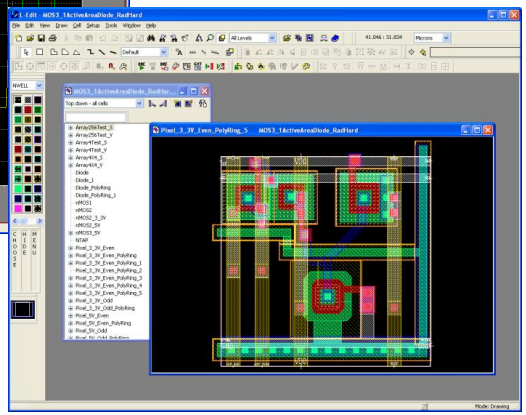
Schematic



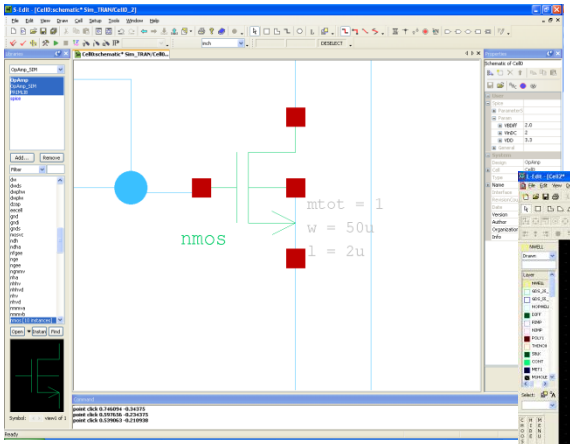


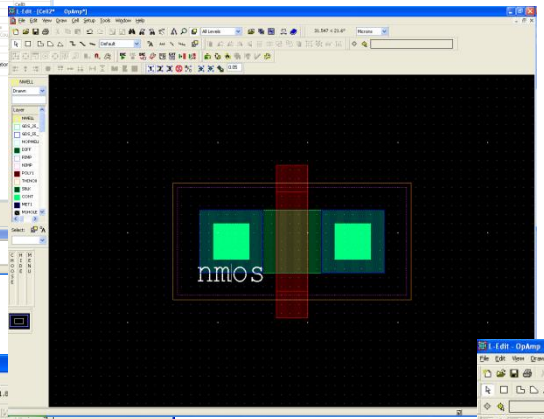
Simulation

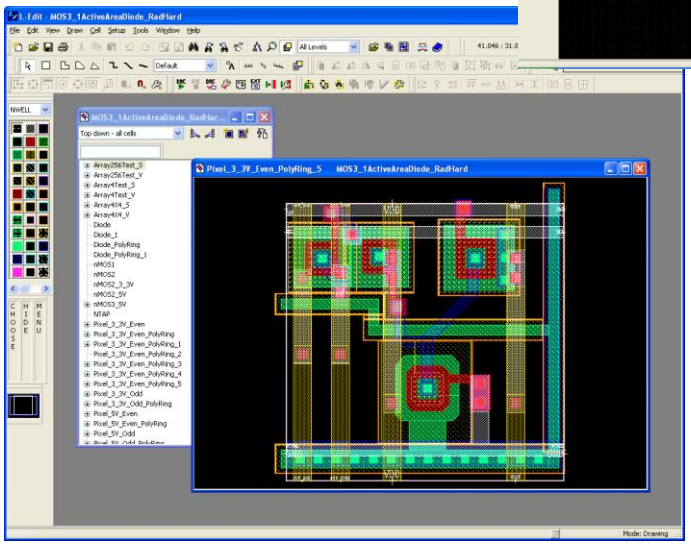
Layout

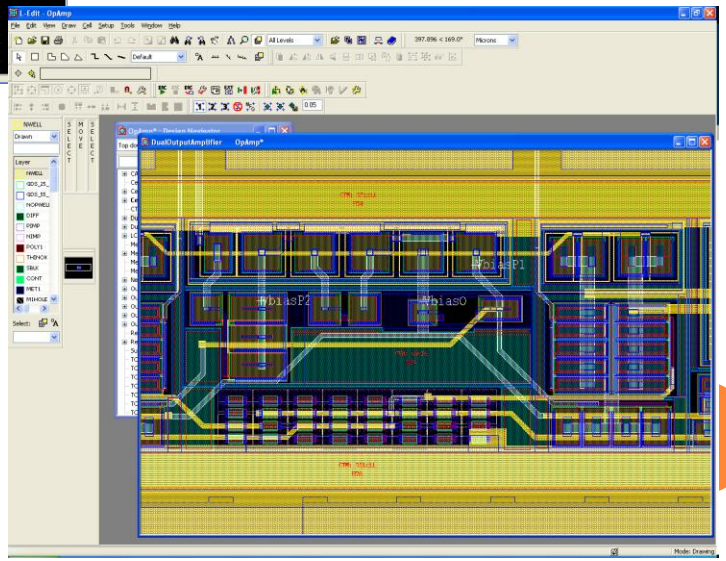


Layout



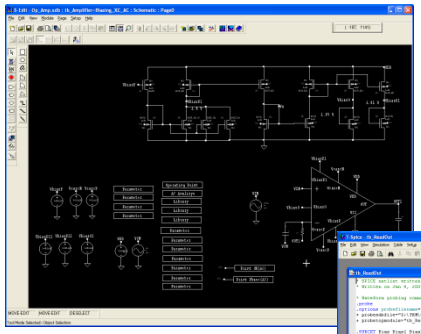




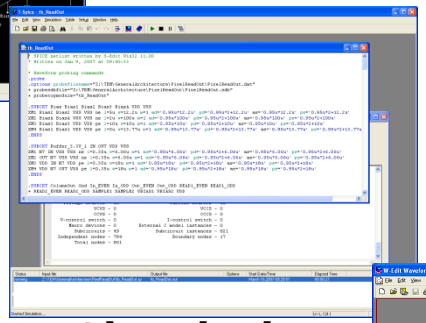


The designed chip has to be “converted” in a format suitable for fabrication.

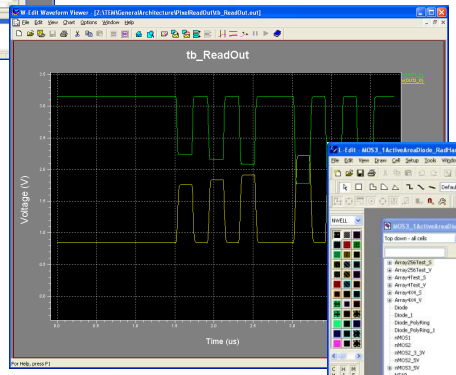
Design Flow



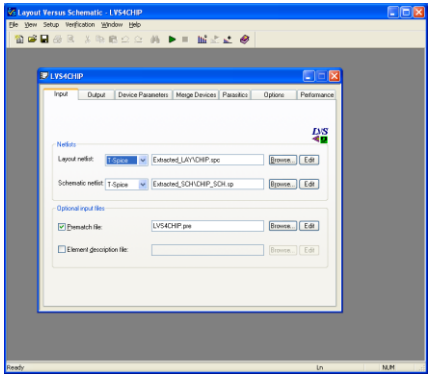
Schematic



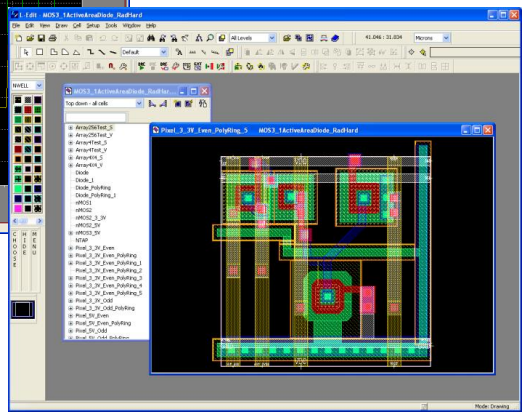
Simulation



Backannotation

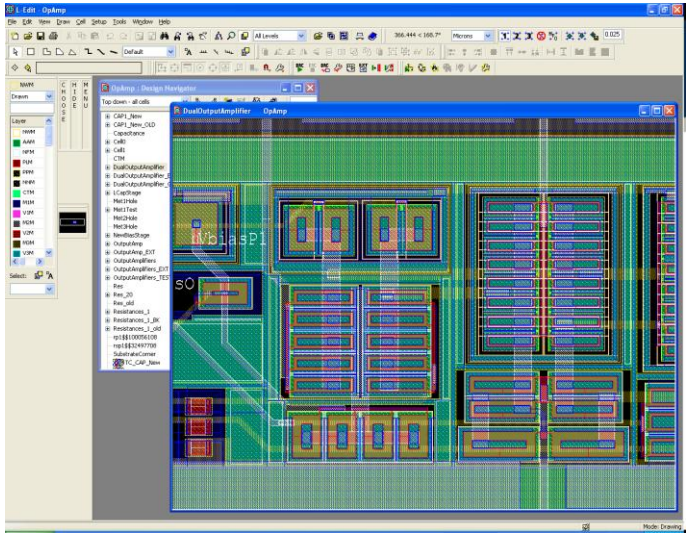


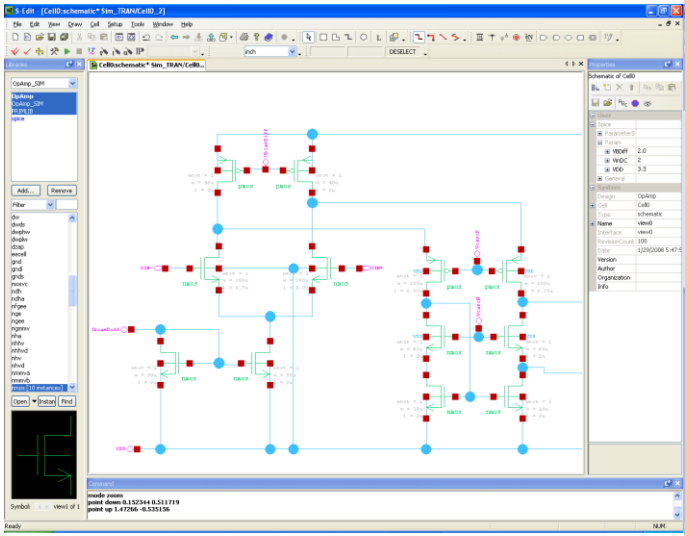
LVS

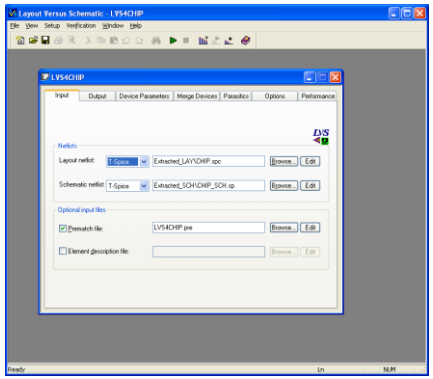


Layout

LVS







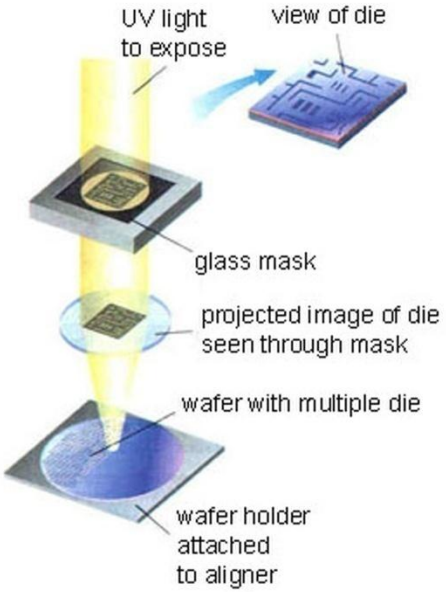
Layout Vs. Schematic compares the designed chip with the file for fabrication

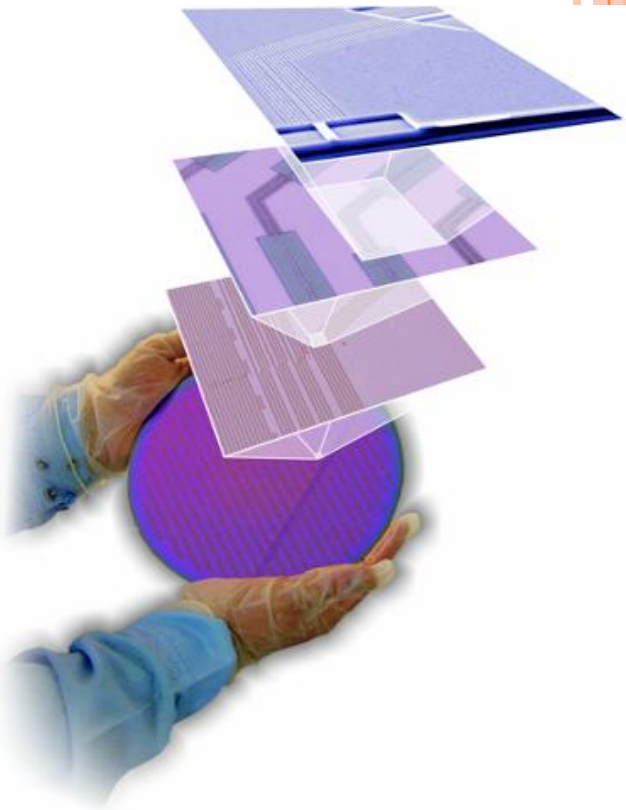
GDS File

The graphical information for the chip fabrication (masks) are stored into a file called a GDS file.

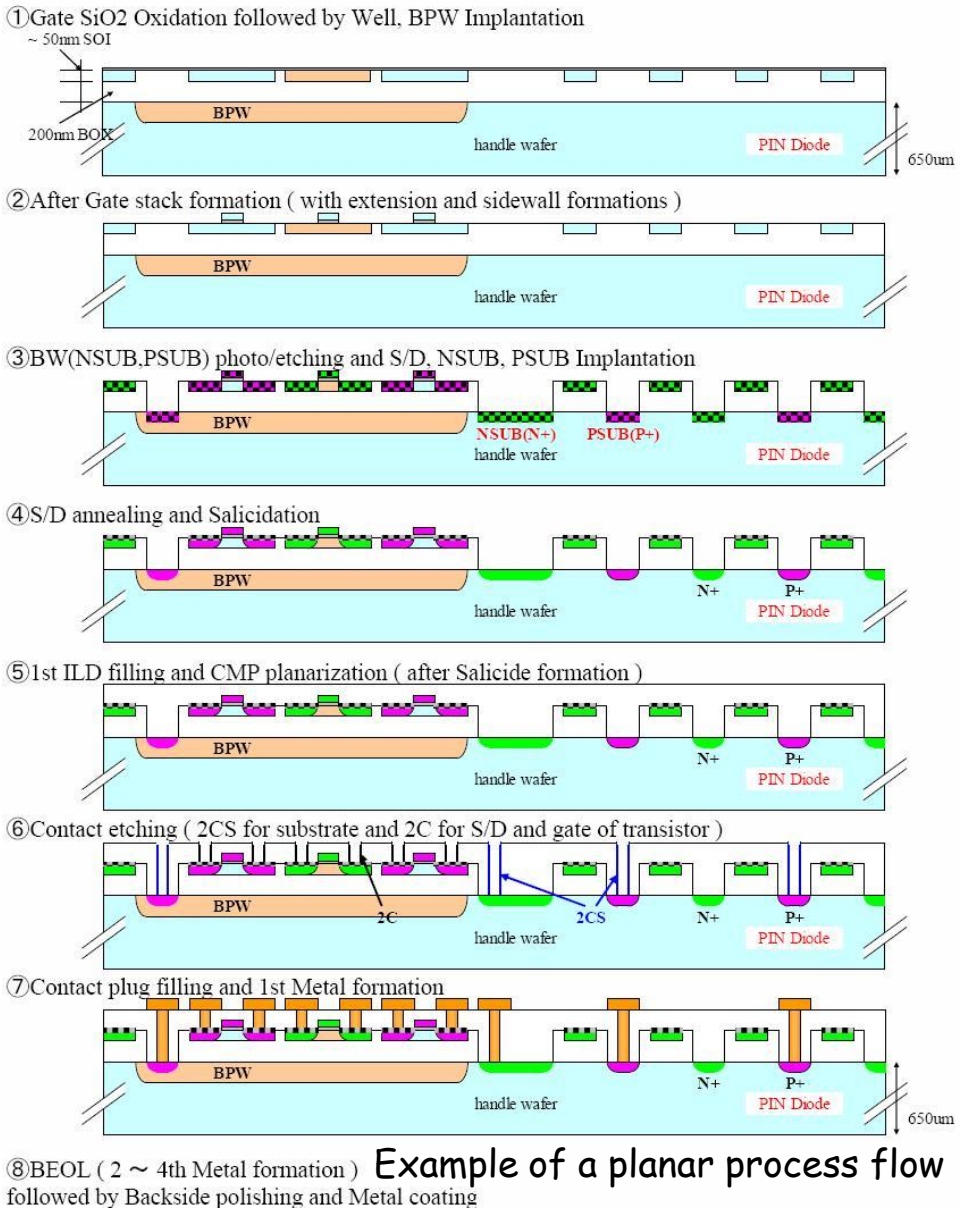
LVS is typically repeated at this stage to ensure the design is correct.

From the information in the GDS file it is possible to fabricate the chip.

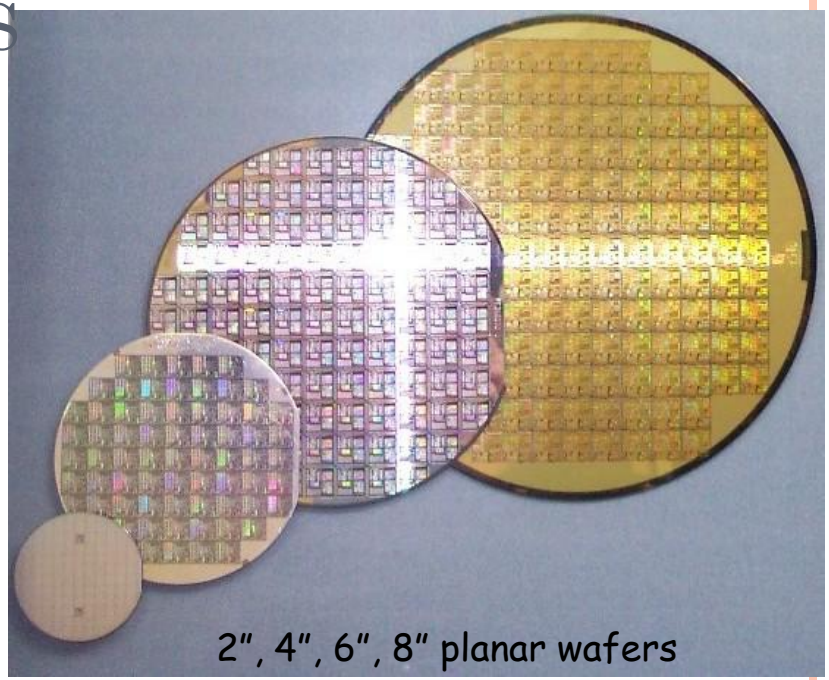




MANUFACTURING PROCESS

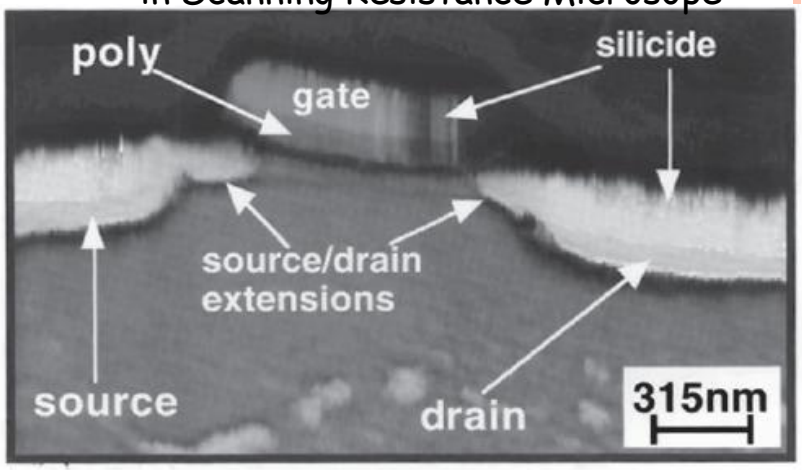


Example of a planar process flow



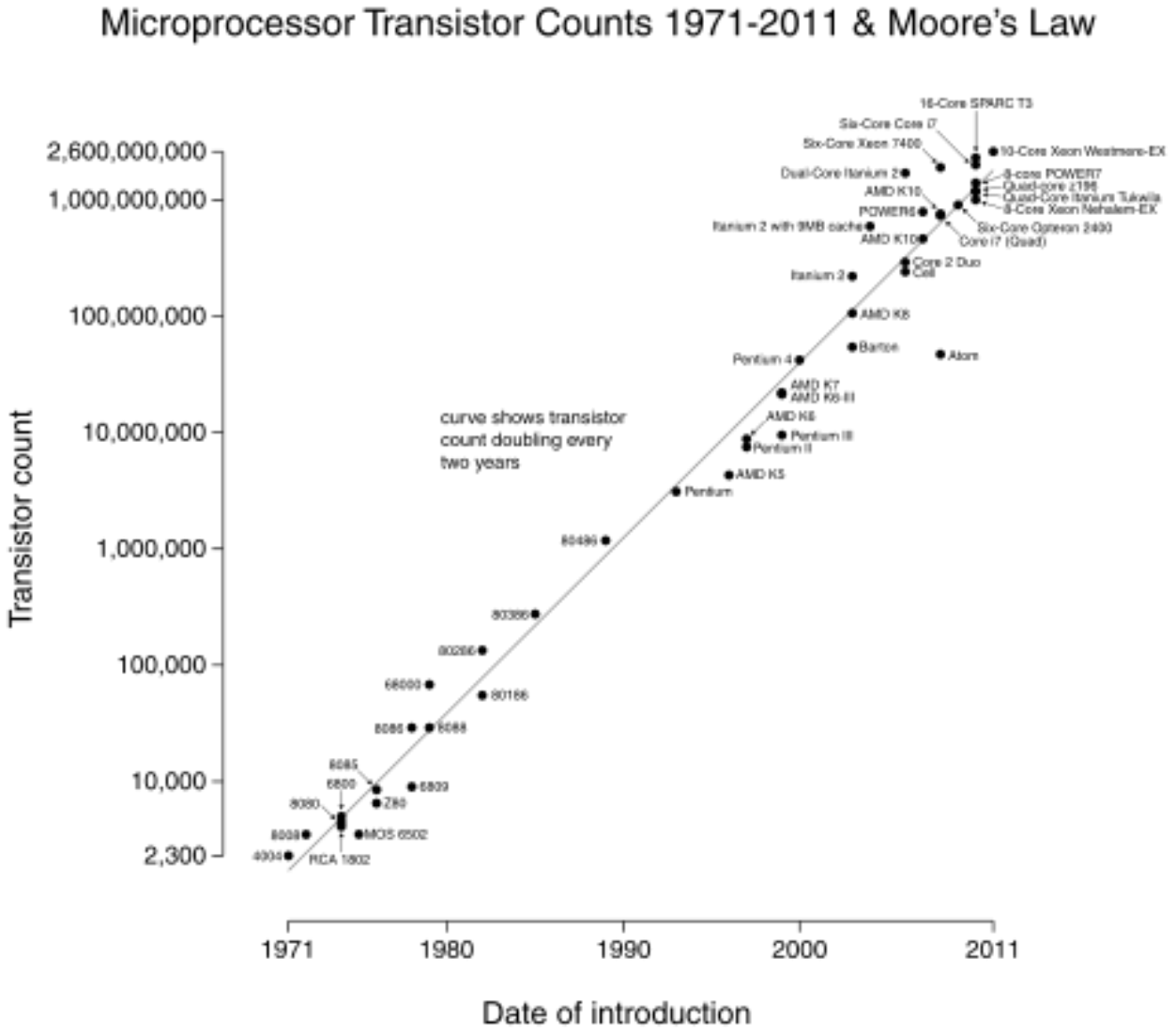
2", 4", 6", 8" planar wafers

X-section of NMOS transistor seen in Scanning Resistance Microsope

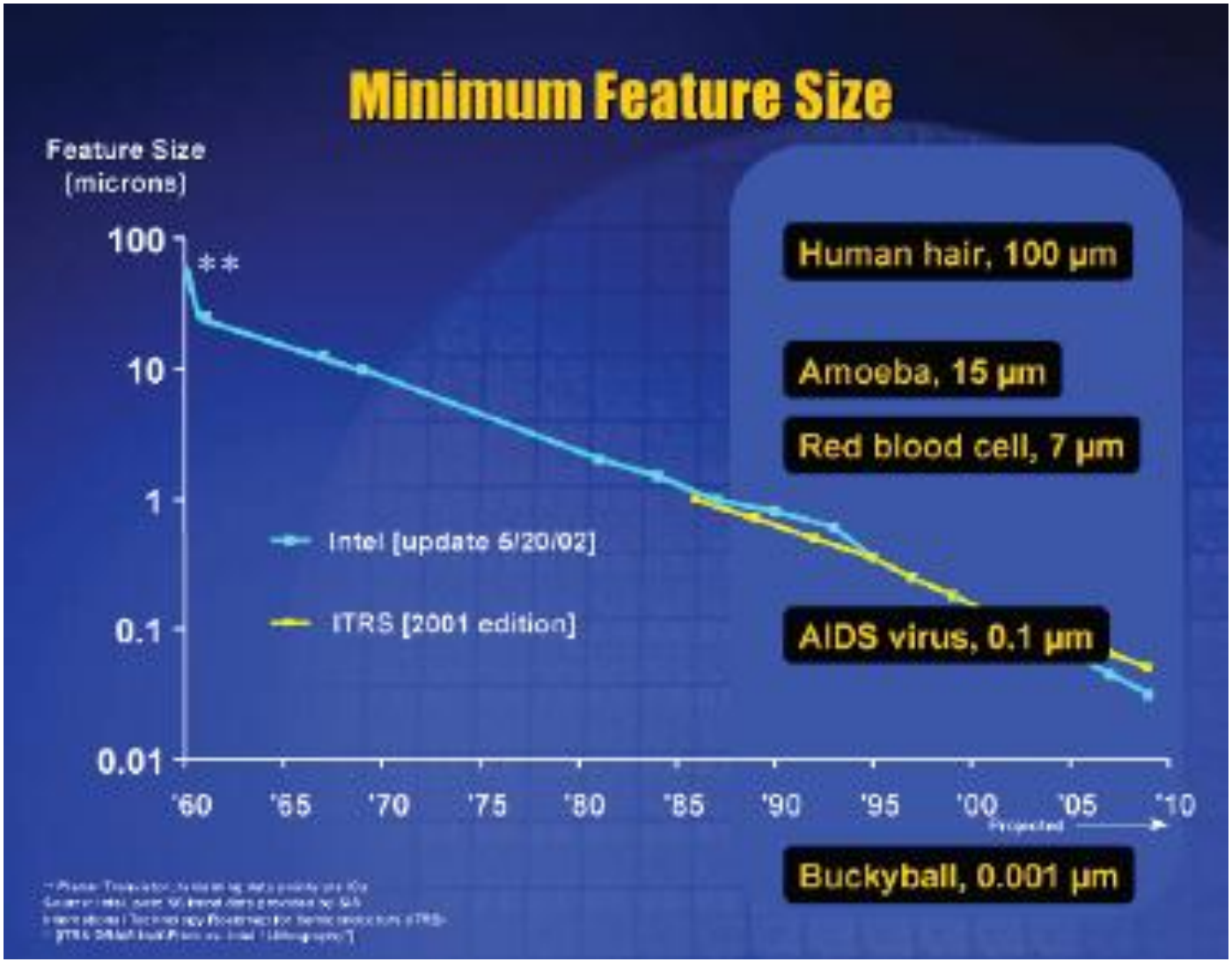


FUTURE

TRENDS: WHAT NEXT?

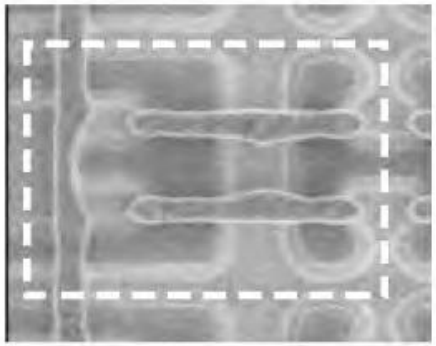


Trends: Transistor size

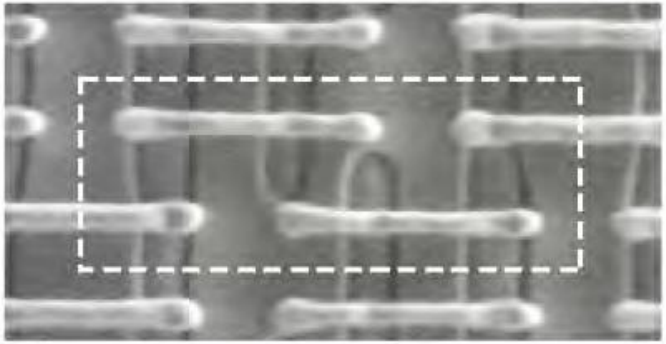


SIZE TRENDS

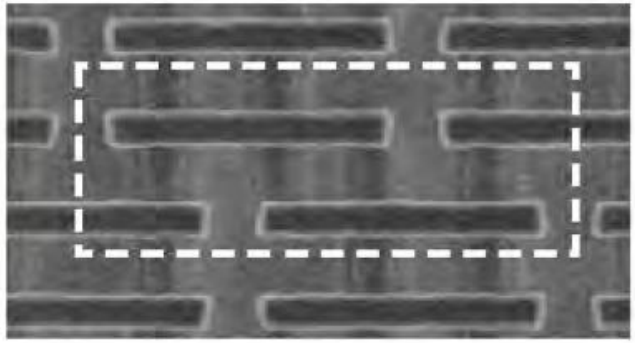
View of the same simple SRAM cell in 90nm, 65nm and 45nm process node



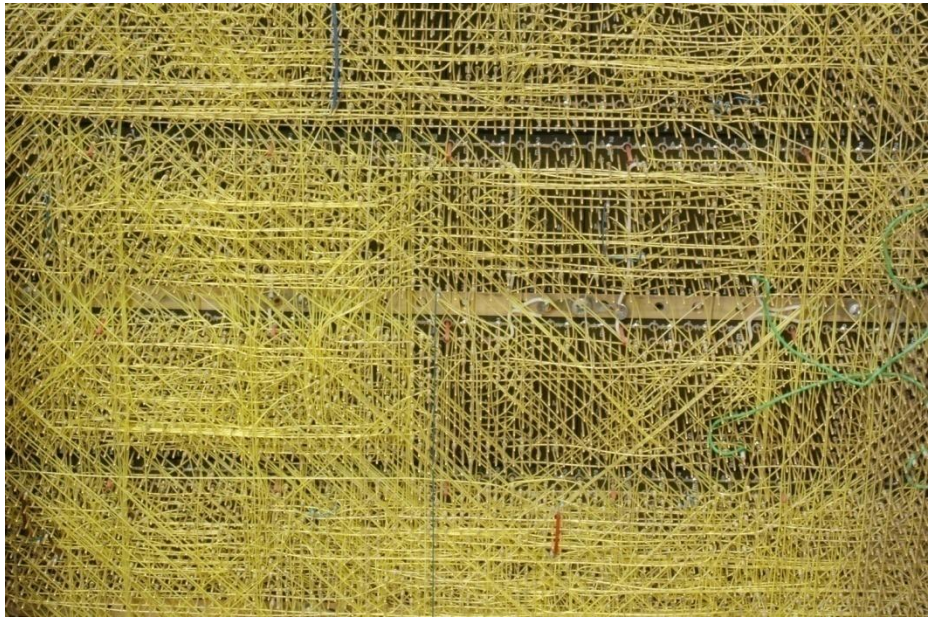
90nm – tall
1.0 μm^2



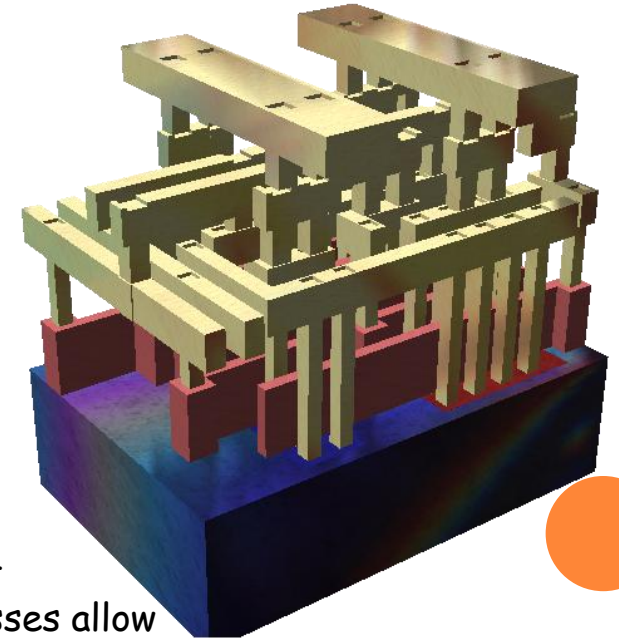
65nm – wide
0.57 μm^2



45nm – wide
w/ patterning enhancement 0.346 μm^2



Interconnectivity is THE ISSUE!!!
Backplane of PDP-8I machine wire-wrapped



recent processes allow up to 10 interconnection metal layers

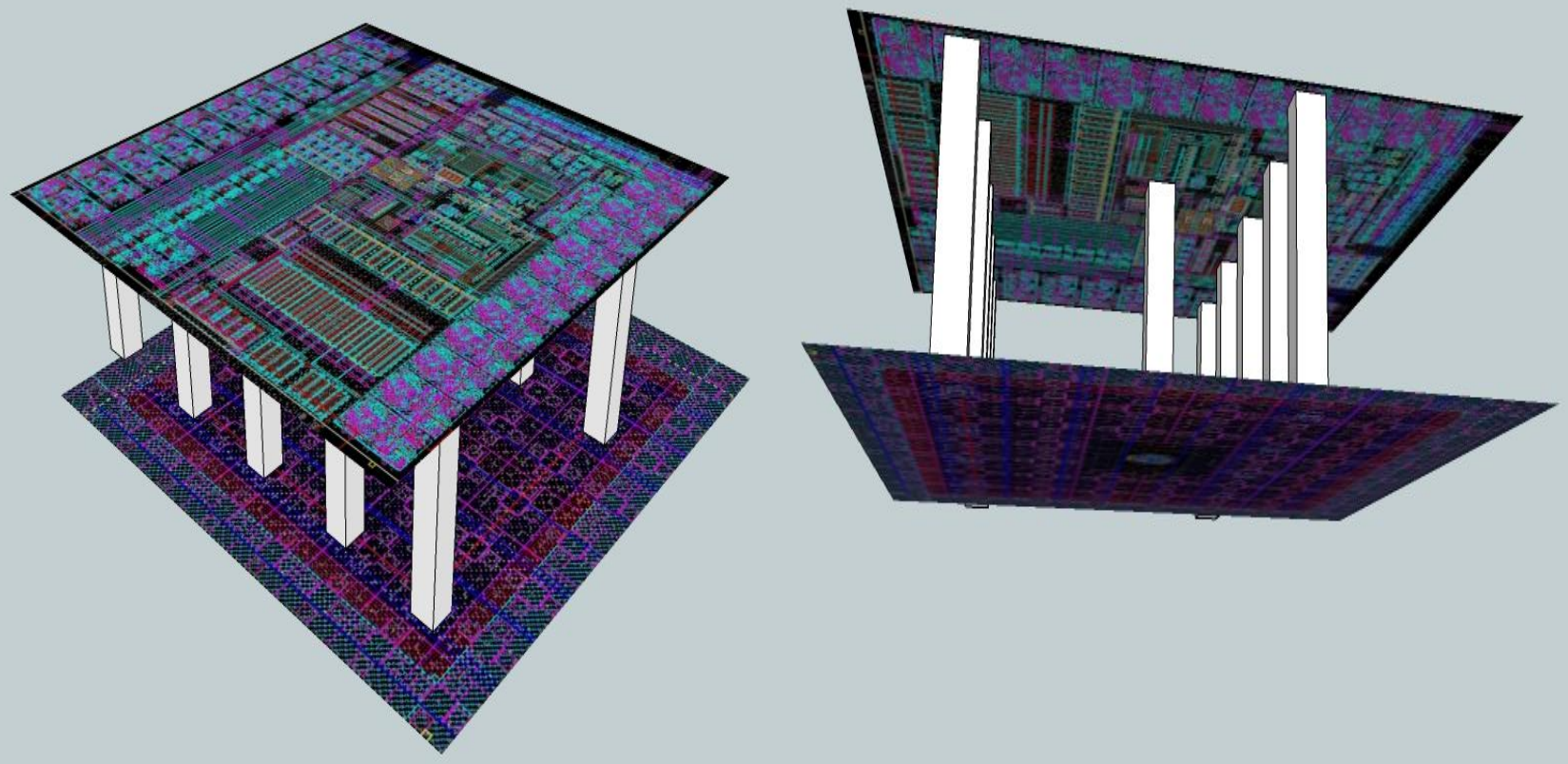
3D IC – Stacking trend

Real estate analogy

How much time, effort and energy (gas) is needed to communicate with your neigbors in 2D assembly?

2D

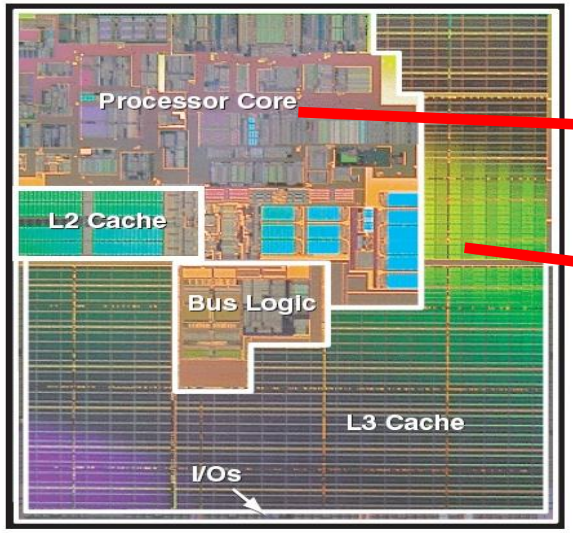
3D PIXEL



Why 3D-IC?

BEFORE Intel Photo used as proxy

Die Photograph of the Itanium 2 MPU
(~2/3 of Area is Cache Memory)



Source: Intel

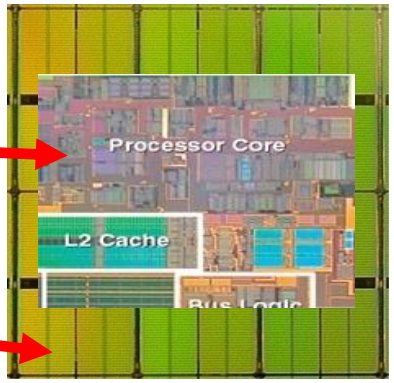
Only memory directly compatible with logic process (virtually no choice!)

maps to logic only die

maps to memory die array

AFTER: 3D IC

rendering of 3D IC



14× increase in memory density
4× Logic Cost Reduction
29× → 100× memory cost reduction (choice!)

Single Die~ 430 mm^2 2D IC "All or Nothing"
Wafer Cost ~ $6,000
Low yield ~ 15%, ~ 10 parts per wafer
memory costs ~ $44/MB

128MB not 9MB
memory costs ~ $1.50/MB → $0.44/MB

Operation	Energy
32-bit ALU operation	5 pJ
32-bit register read	10 pJ
Read 32 bits from 8K RAM	50 pJ
Move 32 bits across 10mm chip	100 pJ
Move 32 bits off chip	1300 to 1900 pJ

Calculations using a 130nm process operating at a core voltage of 1.2V
(Source: Bill Dally, Stanford)

From Bob Patti Tezzaron

Conclusions

- Chips are used everywhere, for a wide range of mundane as well as exotic applications
- Feature size of the transistor has decreased over the decades
- No. of transistors on a single chip has increased over the decades
- New alternates such as 3D stacking is currently being explored to increase functionality of chips

Thank you!

- *Any Questions?*